Magnify the Traditional Mixed-Signal Eyepatch Verification with Aniah

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It is common to find SoC design teams, in the last two months before tapeout, at a crossroads in their efforts to verify large transistor-level netlists. Team managers usually decide to verify correct functionality by running simulations with back-annotated gate-level Verilog along with top-level analog schematic views, black-boxed IOs, and behavioral, time-intensive blocks; we call this common simulation/verification methodology 'eyepatch'. Team managers base their verification decision on balancing the required accuracy and setup limitations to get the tapeout out of the door in time. However, this path is treacherous since communication interfaces, powering schemes, analog-digital boundaries, clock and supply crossing domains verification, among other details, can get overlooked. In fact, you can hear in the design review rooms, team managers demanding old-fashioned careful eyeball checking. The result: a chip prone to undetected flaws and overlooked operational cases that might limit or kill its functionality.

1- Thousands of use cases

From all possible combinations of power states for each block, to the range of application functionality cases, it is hard to claim full coverage using simulation-based techniques. The claim of full coverage gets even harder to believe when you require mixed-signal functionality to be checked. Although eyepatch mixed-signal simulations might limit runtimes to overnight hours, it remains difficult to run all possible cases to avert potential issues before tapeout. Using current tools, you might run verification for months without achieving full coverage.

Usually, the design team independently qualifies analog and digital portions before running mixed-signal simulation. However, operational cases might be overlooked for each portion that might constrain the boundary elements and the mixed-signal operation.

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2- Power-down situations go undetected by eyepatch and eyeball reviews

Common flaws result from overlooked operational cases with an impact on power consumption in mixed-signal circuitry. For instance, Fig. 1. shows a case where some upstream digital blocks, connected to a powered domain (domain 1), might generate a case where IOs can unintentionally leak a large crossbar current. A driver could get enabled by the omission of a correctly powered downstate at the boundary of domains. The question that a design team will raise is: how can I make sure I check all possible cases with my test benches?

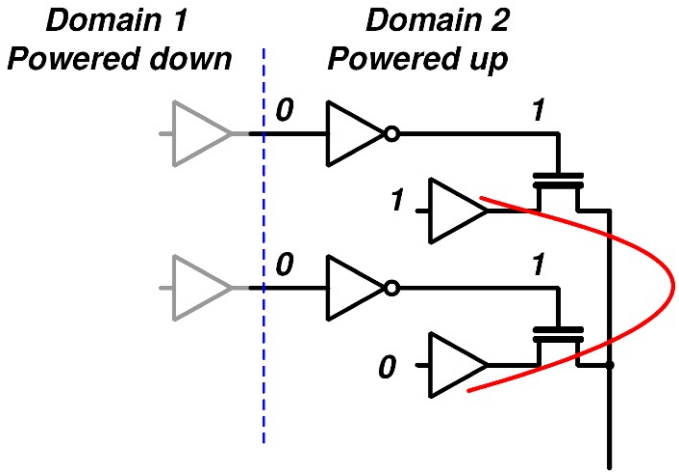

Fig 1. Crossbar current caused by an improper powering scheme at the domain boundary.

Similar cases might occur in powering domains with differential signals. For instance, as shown in Fig. 2, in the case that domain 1 is powered down, both level shifter predrivers would enable both branches of the level shifter causing an undesired crossbar current. We might assume that this type of bug can be fixed by software, for example, by making sure the power down boundaries have proper states before powering down the domain. However, our experience is that many of these cases are overlooked even with the most experienced teams, sometimes causing unintended power consumption in low-power states.

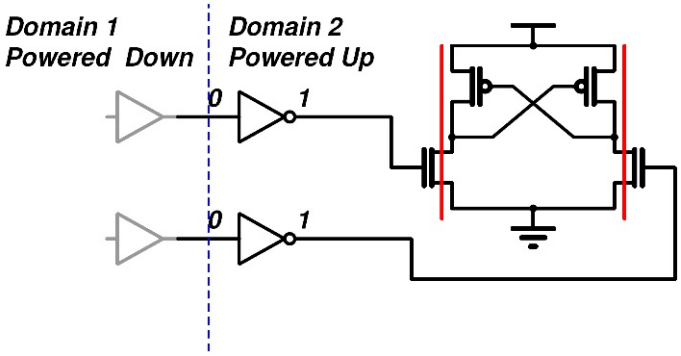

Fig 2. Crossbar currents in differential signaling due to incorrect powering scheme.

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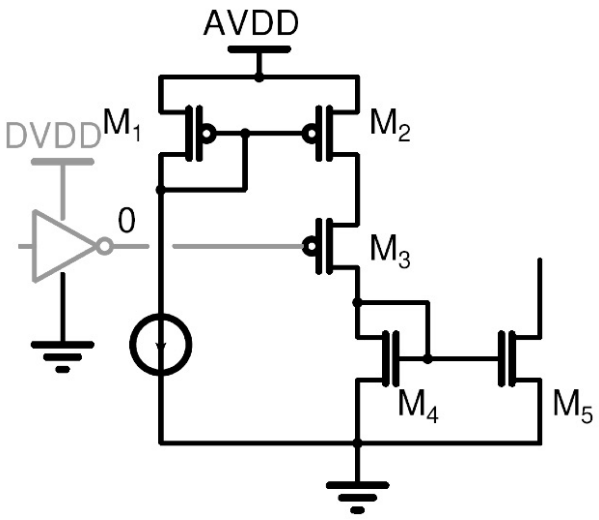

Fig 3. An analog block might be powered even after bias has been disabled.

It is common to have several analog blocks that are biased, and their power controlled by enabling/disabling current mirrors. However, disabling current mirror copies requires proper power-off synthesis. For instance, Fig. 3 shows an inverter driving the copy of the current through M2 branch. By asserting the M3 gate to value logic 1, the M2 branch will be off and M5 becomes zero. However, if DVDD domain is powered off and AVDD still on, M3 may be unintentionally activated. By inserting additional transistors in parallel to pull-up the M3 gate or pull-down the M4 gate, we might disable the current copy even if DVDD is powered off. Here the question is: how can we make sure that we have the proper power-off synthesis in each of the blocks for each power state?

3- Enriching mixed-signal tests with full netlist and reliable Static Electrical Analysis

Eyepatch verification methodology demands complementary tools to eradicate dependency on eyeball checking and reduce undetected mixed-signal interoperation flaws during mixed-signal verification. Reliable Static Electrical Analysis (SEA) tools can run assertion checks from a full netlist in short runtimes to verify electrical errors that might be overlooked by the eyepatch methodology.

Aniah introduces a vector-less electrical verification solution that systematically finds undesired floating nodes caused by power states. Without requiring test benches or input stimulus, Aniah provides built-in assertions to ensure that all potential use cases are verified against undesired electrical flaws or conditions.

Aniah goes through a full netlist and qualifies all possible states, reducing the likelihood that electrical errors go undetected. All possible states are verified no matter how the analog/digital split is structured. Built-in assertions will make sure there is a proper power-off synthesis in each of the blocks for each power state of the full SoC without impacting verification runtimes.

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Today there are various methodologies for the verification of a SoC using Analog Mixed Signal (AMS) approaches, but they still rely on behavioral or descriptive models and do not cover the final product: LVS netlist + GDS file. Additionally, the absence of equivalence checkers between analog circuit simulation and functional behavioral models, if the inherent errors lie in model abstraction, opens the door to blind spots in verification and jeopardizes first silicon success.

In Fig. 4 (a) a traditional AMS verification methodology is compared with the Aniah Power Aware SEA tool. While AMS verification has some blind spots (those stages not colored in green), by using Aniah SEA, verification is ensured even in the early design stages.

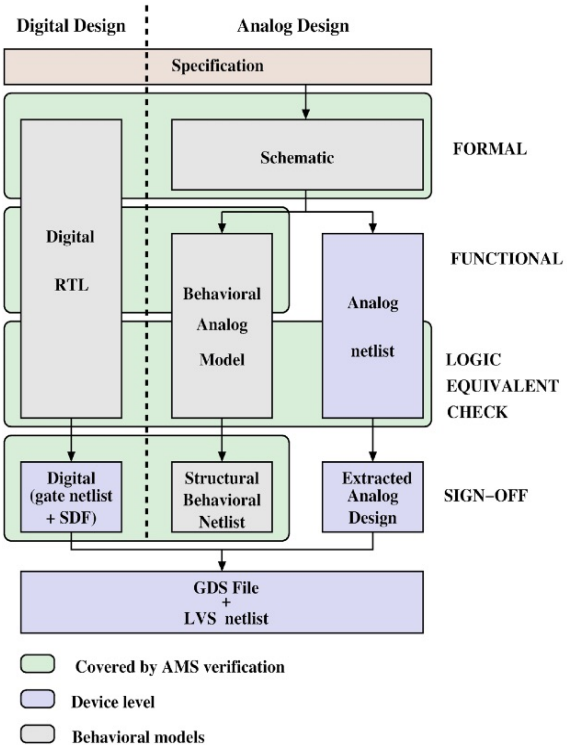

Fig 4. (a) Analog Mixed Signal Verification Methodology.

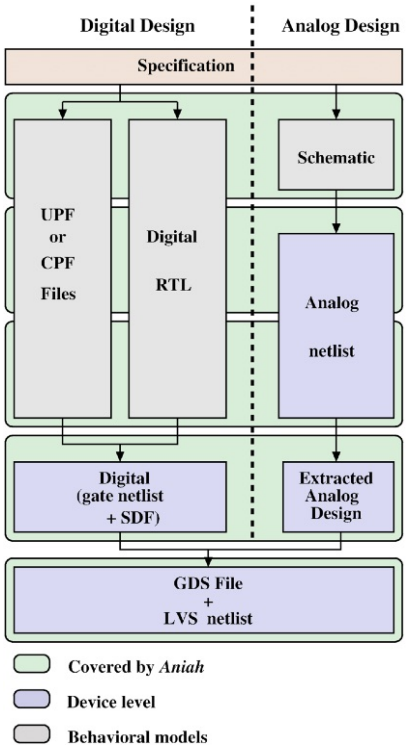

Fig 4. (b) Complementary methodology using Power Aware SEA tool available from Aniah

4- Conclusion

Unlike mixed-signal tests, Aniah does not require multiple testbenches, boundary elements setup, long runtimes, and dense waveform processing to perform electrical diagnostics on the analog-digital stitching. Aniah performs SEA checking as a standalone tool with a flat or hierarchical full netlist. Aniah complements mixed-signal verification, eliminating the risk of undetected corner cases. If you are planning mixed signal verification, trying to hit some coverage closure with eyepatch methodology, you can get quick peace of mind before tape-out with Aniah. Aniah takes your full netlist with billions of devices and with thorough built-in assertions, verifies that correct electrical functionality holds.

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