Electrical errors in ICs: why they occur and their consequences

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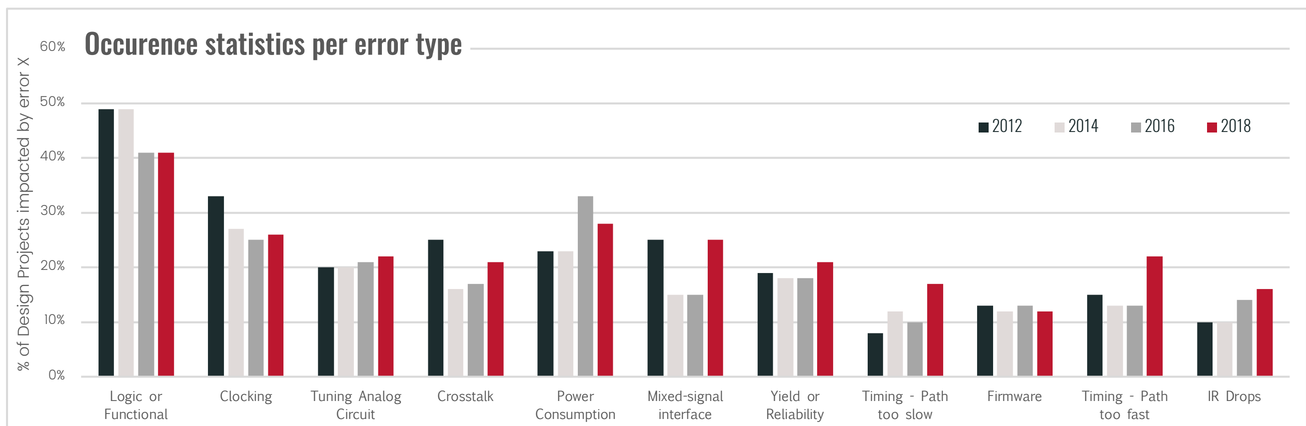
The verification of electrical errors at chip-level has always been the missing step in chip design closure – even though a chip is, basically, a very large circuit. The complexity of such an analysis has so far made it impossible.

Consequently, considerable effort is made throughout the design flows to avoid electrical errors from occurring in the first place. Experience, however, shows that without a verification solution dedicated to the analysis of electrical circuits at the chip scale, some errors elude the vigilance of design engineers, even with the most comprehensive design flows.

Those errors have severe consequences, ranging from delays in the project schedule (thus increasing its cost), failed time-to-market and in the worst case, product recalls (and the major financial as well as brand image impacts this can imply).

In this document, we go over why chips routinely go to fab with undetected electrical errors and the consequences that such errors have on a chip project success and lifetime.



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1- Electrical errors without a full-chip, full-coverage verification solution

1.1 Thousands of power states

A chip typically includes many IPs and macrocells: monitoring, regulators, PHYs, application-specific analog circuitry, a variety of independent digital blocs, etc. With power consumption in mind, each can be turned on and off independently.

The combination of each individual power state at chip level results in thousands of power scenarios. IP designers must include this constraint directly in their design, while top level integrators must account for on and off constraints for each bloc. The sheer number of combinations makes it impossible to consider each individual case – and makes it difficult for simulation-based techniques to go through all possibilities.

We can illustrate this point with the example of an audio-on-USB behavior with a damaged-cable scenario, where the USB signals are shorted with the power line. In this case, the 5V signals leak to the audio amplifier 3.3V supply, then backwards through the regulators and battery charger to the battery itself – possibly damaging the battery.

1.2 Electrical interface specification consistency

Another cause of electrical errors in ICs is an error in IP specifications. In such a case, the integration of the IP leads to errors. The certification process of an IP is usually dimensioned to avoid such issues. However, errors often occur with last-minute-change of the IP to adapt to new integration constraints.

A simple example of such an error is the inversion of the rise sequencing of the digital and analog supplies from one IC to the next. Such constraint, if not explicitly specified, would lead to a significant leakage in standby modes.

The large number of IPs integrated in ICs and variety of power states increases the occurrence probability of such errors.

1.3 Interface between analog and digital blocs

In mixed-signal designs, the number of signals crossing the analog-digital boundaries can be large, including many feedback loops. For instance, a power-on-reset signal from the analog domain that advances a state-machine in the digital domain, which in return boots the bandgap and regulator analog blocs.

The functionality is split between both domains and makes a failsafe packaging and certification of both parts difficult. Especially as they are often designed concurrently and may evolve after close to the design closure phase.

The likelihood of electrical inconsistency in such cases is further increased with sandwiched analog IPs, where signals are tunneled through digital to the analog part. Mixed-signal verification is key to avoiding errors, but the complexity of such analysis may however limit coverage of all possible scenarios.

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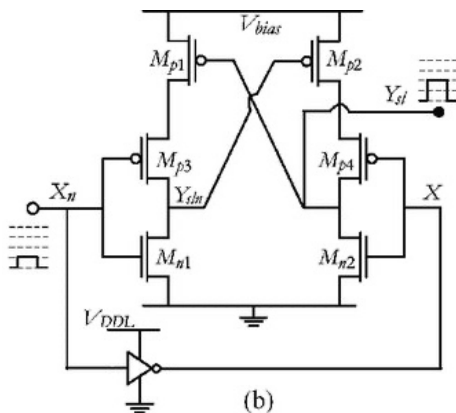
1.4 Limited description of electrical behaviors in abstract views

Some specific constraints may not be described in digital-targeted abstract views of IPs or cells. An example of such a case would be a signal value's relationship with the power states to avoid high-impedance nets in the analog circuitry.

Consequently, the implementation tools cannot account for this constraint, which again may lead to electrical errors.

1.5 Implementation flow robustness

Implementation flows must be adapted to new process constraints that leads to massive errors. The advanced biasing techniques available to FD-SOI designs illustrate this need for the integration of electrical constraints throughout the implementation flow.



1.6 Non-systematic errors

Analog simulators may fail to detect errors when bi-stable conditions can exist in analog circuitry. Common level shifters with their input stage supply off exhibit this condition. More complex cases have been reported in 'off' analog topologies in specific process / temperature conditions.

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2- Consequences of ERC errors

2.1 Lack of functionality

Electrical consistency errors can result in defective functionality. Boot lock-up condition is the most spectacular of such errors, where a chip cannot boot because of impossible conditions between boot signals or clocks and available voltages. Another example is a missing level shifter between domains with a large voltage gap.

Then, a metal fix or even a full mask respin is necessary, with cost and delay consequences on the project.

In a more covert and thus dangerous way, the functionality impact may be specific to a corner usage case. A leakage in a substrate diode in an audio amp at maximum amplitude may not be immediately detected but is likely to have a strong impact on a project schedule.

2.2 Current leakage

The most common consequence of electrical errors is an excessive current consumption, especially harmful in low-power mode. This failure mode comprises all low-gap domain crossing errors, some high-impedance nets, and parasitic forward-biased diodes.

2.3 Reliability

2.3.1 Electrical overstress

Usage of low-voltage devices in higher-voltage domains results in device breakdown, either directly or over time. The failure to identify all weak spots has been known to lead to catastrophic product recalls and may also endanger a project's schedule in case of a detection only during late qualification stages.

Stress conditions may occur only during production test, where the chip is used in test modes not considered in reliability qualification. This stress can create weaknesses and shorten a chip's lifetime. This is made more likely when stress needs to be applied during test to expose early failure defects: one needs to make sure that only early failures are triggered so that the lifetime of the chip is not impacted.

2.3.2 Electrostatic discharge

The protection policies against electrostatic discharges, either Human Body Model or Charged Device Model, have strengthened as the process advances have made devices more sensitive. The 3D stacking and complex packaging also increase the risk of ESD failures with higher pin count (in the millions) and pads spread across the die area.

2.3.3 NBTI / HCI / electro migration

Conditions that lead to degradation of performances over time are highly design dependent for NBTI, HCI and electromigration. Ageing simulation has been seen to fail to detect ageing

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stress that occurs in specific power scenarios in analog circuitry. In addition, the consequences of degradation over time of any single device at system level are complex to predict.

2.3.4 Thermal breakdown

Transistor-scale self-heating effects may lead to temperature-induced breakdowns. A rigorous analysis of such effects requires an accurate joint analysis of both the electrical circuit and its thermal counterpart - both containing billions of elements.

2.3.5 Random errors

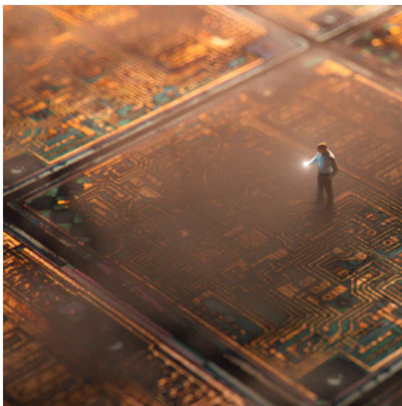
The impact of non-systematic or external-condition-dependent errors may be considered as the worst of electrical consistency errors, as they will become discovered late in the project, possibly in the final qualification stage or during on-field testing.

High-impedance nets range high in such errors as they may settle to different levels depending on 2nd order effects such as off currents and thus not be accounted for in the circuit analysis. The case of bi-stable circuits mentioned above is also likely to result in unpredictable behaviors.

Many of the worst ramp-up crises are due to those dangerous errors.

3- Full-chip electrical verification is a must

Considering the occurrence frequency and massive impact of electrical errors on IC designs, we believe that an increased focus on electrical verification will be more and more critical as ICs and SOC continue to become more and more complex.



Aniah has introduced an electrical verification solution that tackles the issue at the scale of the largest chips, with a runtime in minutes for billion-devices circuits.

Aniah has developed a breakthrough tool that enables an electrically accurate analysis at chip level, focusing on the above-mentioned errors to suppress their impact on IC design projects.

Our first results on large chips have proven that this goal can be attained.

Please contact us for more information on how to deploy our solution in your design flows.

4- Conclusion

While the consistency of design flows, adherence to best practices for design and Silicon qualification techniques significantly reduce the likelihood that electrical errors may go undetected in mass production, the absence of a full-coverage verification technique; the delays resulting from additional silicon spins and the possible cost of customer recalls, make electrical errors a significant risk in chip design.

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